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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,998	09/30/2003	Ole Agesen	A34	7241

7590 10/11/2006

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EXAMINER	
INGBERG, TODD D	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,998	AGESEN, OLE	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *12-16* is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/30/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 16 have been examined.

Information Disclosure Statement

1. The Information Disclosure Statement filed November 17, 2003 has been considered.

Drawings

2. The drawings filed September 30, 2003 have been accepted.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation ***"substantially uniformly"*** has no quantifiable meaning.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 11 are rejected under 35 U.S.C. 102(b) as being anticipated by "Improving Prediction for Procedure Returns with Return-Address-Stack Repair Mechanisms, by Kevin **Skadron** et al, IEEE, 1998, pages 259 – 271.

Claim 1
A method for implementing subroutine calls and returns in a computer system comprising the following steps:

A) converting a sequence of input language (IL) instructions into a corresponding sequence of output language (OL) instructions;
B) executing the OL instructions;
C) for each call to an IL subroutine made from an IL call site in the IL instruction sequence:
i) storing a call site IL return address Rcall on a stack;
ii) calculating a first index by evaluating a function with P as an argument, where P is a procedure entry address of the subroutine;
iii) storing a corresponding OL return address in a return target cache at a location indicated by the first index;
iv) executing an OL subroutine translation of the called IL subroutine;
D) upon completion of execution of the OL subroutine translation,
i) in a launch block of instructions, retrieving an OL target address from the return target cache at the location indicated by a second index; and
ii) continuing execution beginning at the OL target address.

Examiner's Rejection

A. Set up for prediction for Procedure Returns (Skadron, page 260, Abstract).
B. Program runs
C. set up for each path (Skadron, page 268, right side establish a private copy of the return-address stack for each path).
D. Upon return check to see which path to take (As per C above paths saved in private copy of return-address stack – Table 8 shows most efficient technique present).
See Figure 4.

Claim 2

A method as in claim 1, further including the following steps: determining whether a predicted IL return address RPred is the same as an actual IL return address Ractual, fetched from the stack and, if it is not, transferring execution to a back-up OL return address recovery module; and
in the back-up OL return address recovery module, establishing the OL return address using a predetermined, secondary address recovery routine.

Examiner's Rejection

Step D of claim 1 – takes the path required.

Claim 3

A method as in claim 2, in which there is a plurality of IL call sites, further including the following steps:
translating each IL call site into a corresponding OL call site; generating a confirm block of instructions corresponding to each OL call site; upon execution of any confirm block of instructions: comparing the actual IL return address Ractual with the predicted IL return address RPred; if Ractual is equal to Rpred, continuing execution of the OL instructions following the OL call site; and if Ractual is not equal to Rpred, transferring execution to the back-up return address recovery module.

Examiner's Rejection

The confirm block is considered the inherent overhead in the system to perform the basic check of any of the techniques present. The back-up address recovery module is the private copy of claim 1.

Claim 4
A method as in claim 3, in which only a single scratch register is used for the in the launch and confirmation blocks of instructions.
Examiner's Rejection
Skadron Page 269, left side – stack implements "pointer & data" fix up after mis-predictions.

Claim 5
A method as in claim 3, in which: the return target cache is an array having a plurality of elements; the function maps IL return addresses substantially uniformly over the return target cache; equality and inequality between Ractual, and Rpred are defined as a hit and miss, respectively; further including the following steps:
calculating a return success measure as a function of the frequency of occurrence of hits relative to the frequency of occurrence of misses; adjusting the number of elements in the return target cache according to a function of the return success measure.
Examiner's Rejection
Skadron, page 270, Table 8 shows statistics captured.

Claim 6
A method as in claim 2, in which the return target cache is an array having a plurality of elements, further including the step of initializing the return target cache by storing in each element a beginning address of the back-up return address recovery module.
Examiner's Rejection
(Skadron, page 268, right side establish a private copy of the return-address stack for each path – requires the address for each path to be part of the return-address stack).

Claim 7
A method as in claim 1, in which: the return target cache is an array having a plurality of elements; and the function maps IL procedure entry addresses substantially uniformly over the return target cache.
Examiner's Rejection
(Skadron, page 268, left side – structure of per path stacks would constitute a multidimensional array. The stored structures are private copies of return-address stack for each path.

Claim 10
A method as in claim 1, further comprising binding a translation of a return within the OL subroutine translation to an index in the return target cache.
Examiner's Rejection
(Skadron, page 268, left side –The stored private copies of return-address stack for each path require a technique to retrieve the proper path. The reference is not explicit how the index is built. This explains the allowable subject matter below.

Claim 11
A method as in claim 10, further comprising: setting a specified entry of the return target cache a predetermined value indicating a lack of binding; and upon sensing attempted access to the specified entry of the return target cache, scanning the return target cache and associating with the current unbound launch block an array index other than the specified index.
Examiner's Rejection
The matching of the proper path with the value returned as per Skadron, page 268 right side.

Allowable Subject Matter

7. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art of record teaches several techniques for prediction for procedure returns. Prior art of record fails to explicitly disclose the indexing technique of the stored information to ensure the proper path is taken. In claim 8 the technique of "return target cache is identified by an array index, and the function extracts a number of bits from the address P" is not taught. And in Claim 9 the limitations of "calculating the first index k is performed as part of the step of converting the IL call into the corresponding sequence of OL instructions". the prior art does teach the use of bits for history on page 260 of Skadron. the two bit counter is associated with branch target buffer entries. The reference is silent as to the use of the association as an index.

Claim 8
A method as in claim 7, in which each of the elements of the return target cache is identified by an array index, and the function extracts a number of bits from the address P.

Claim 9
A method as in claim 1, in which the step of calculating the first index k is performed as part of the step of converting the IL call into the corresponding sequence of OL instructions.

8. Claims 12 – 16 are allowed. For the same reasons as for claims 8 and 9 above.

Furthermore, claims 12 on teach the interaction of the host and guest machine which is a form of virtualization.

Claim 12
A method for implementing subroutine calls and returns in a computer system comprising the following steps:
A) converting a sequence of input language (IL) instructions of a guest system into a corresponding sequence of output language (OL) instructions of a host system;
B) executing the OL instructions in the host system;
C) for each call to an IL subroutine made from any of a plurality of IL call sites in the IL instruction sequence:
i) translating each IL call site into a corresponding OL call site;
ii) storing a call site IL return address Ra,, on a stack;
iii) calculating a first index by evaluating a function with P as an argument, where P is a procedure entry address of the subroutine;
iv) storing a corresponding OL return address R' in a return target cache at a location determined by the first index, the return target cache comprising an array of elements;
v) executing an OL subroutine translation of the called IL subroutine;
D) upon completion of execution of the OL subroutine translation,
i) retrieving an OL target address from the return target cache at the location indicated by a second index; and
ii) continuing execution beginning at the OL target address
E) generating a confirm block of instructions corresponding to each OL call site and, upon execution of any confirm block of instructions:
i) comparing an actual IL return target address Ractual fetched from the stack with the predicted IL return address Rpred,
ii) if Ractual is equal to Rpred, continuing execution of the OL instructions following the OL call site; and
iii) if Ractual is not equal to Rpred, transferring execution to the back-up return address recovery module; and
F) in the back-up return address recovery module, determining a correct OL return address.

Claim 13
A method as in claim 12, further comprising binding a translation of a return within the OL subroutine translation to an index in the return target cache.

Claim 14
A system for implementing subroutine calls and returns in a computer system comprising:
A) a host computer system that executes host instructions in an output language OL;
B) a guest system that is operatively connected to the host system and that issues a sequence of instructions in an input language (IL) including a call to a subroutine;

C) a binary translator converting the sequence of input language (IL) instructions of the guest system into a corresponding sequence of the output language (OL) instructions of the host system and storing the OL instructions in a translation cache,
D) the binary translator comprising computer-executable instructions for translating an IL subroutine call and an IL subroutine return into corresponding OL instruction sequences, including a call block and a launch block of OL instructions;
E) the call block, upon each call to an IL subroutine from an IL call site in the IL instruction sequence, comprising computer-executable instructions

i) for storing a call site IL return address Rcall of the call on a stack;

ii) for determining a first index by evaluating a function with P as an argument, where P is a procedure entry address of the subroutine; and

iii) for storing a corresponding OL return address R' in a return target cache at a location determined by the first index;

iv) for transferring execution to the OL subroutine translation of the called IL subroutine;
F) the launch block, upon completion of execution of the OL subroutine translation, further comprising computer-executable instructions

i) for popping an actual IL return address Ractual the stack;

ii) for retrieving an OL target address from the return target cache at the location indicated by a second index; and

iii) for continuing execution beginning at the OL target address.

Claim 15
A system as in claim 14, in which: there is a plurality of IL call sites; the binary translator comprises computer-executable instructions for translating each IL call site into a corresponding OL call site; for inserting a confirm block of instructions into each OL call site; for comparing Ractual,with a predicted IL return address Rpred corresponding to the current OL call site; for continuing execution of the OL instructions following the OL call site if Ractual, is equal to RPred; and for transferring execution to the back-up return address recovery module if Ractual is not equal to Rpred.

Claim 16
A system as in claim 14, in which the binary translator comprises further computer-executable instructions for binding a translation of a return within the OL subroutine translation to an index in the return target cache.

Correspondence Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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